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**National Universityof Computer and Emerging sciences**

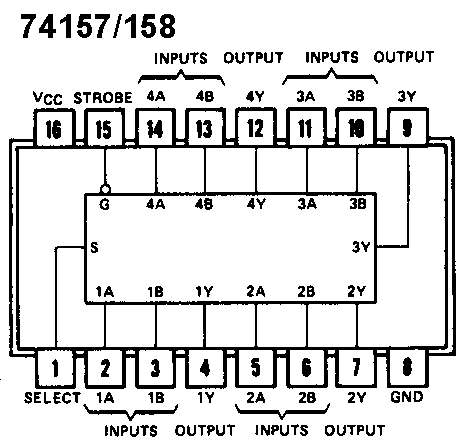
**Objectives:**

* To learn the implementation of Boolean function using multiplexer
* To learn how to implement Multiplexers using decoders

**2x1 MUX:**

74LS157 IC is a dual 4x1 MUX with active low enable.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **STROBE (Enable)** | **SELECT** | **A** | **B** | **Y (o/p for LS157)** | **Y (o/p for LS158)** |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

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**4x1 MUX:**

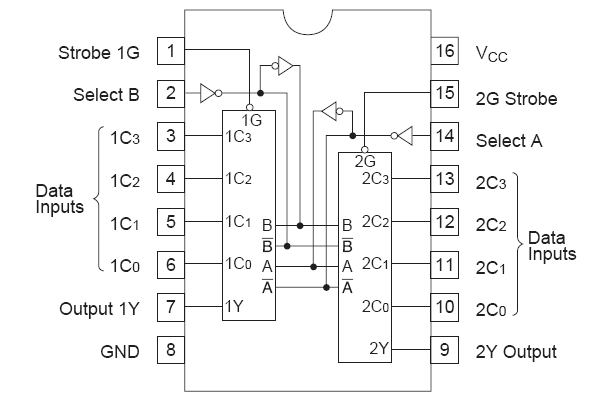
74LS153 IC is a dual 4x1 MUX with active low enables. Two 4x1 MUXs with common selection pins but independent inputs and independent outputs is known as dual 4x1 MUX. The function table and connection diagram for this IC are shown below:

**Function Table:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Strobe (Enable)** | **Selection Inputs** | | **Data Inputs** | | | | **Output** |
| **G** | **B** | **A** | **C0** | **C1** | **C2** | **C3** | **Y** |
| **H** | **X** | **X** | **X** | **X** | **X** | **X** | **L** |
| **L** | **L** | **L** | **L** | **X** | **X** | **X** | **L** |
| **L** | **L** | **L** | **H** | **X** | **X** | **X** | **H** |
| **L** | **L** | **H** | **X** | **L** | **X** | **X** | **L** |
| **L** | **L** | **H** | **X** | **H** | **X** | **X** | **H** |
| **L** | **H** | **L** | **X** | **X** | **L** | **X** | **L** |
| **L** | **H** | **L** | **X** | **X** | **H** | **X** | **H** |
| **L** | **H** | **H** | **X** | **X** | **X** | **L** | **L** |
| **L** | **H** | **H** | **X** | **X** | **X** | **H** | **H** |

H= Logic High, L= Logic Low, X= Don’t Care

**Connection Diagram:**



**2-to-4 line decoders:**

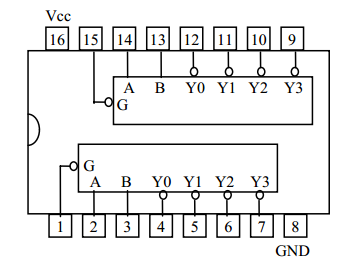
74LS139 IC contains two fully independent 2-to-4 line decoders with active low enables. The function table and connection diagram for this IC are shown below:

**Function Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Enable** | **Selection Inputs** | | **Outputs** | | | |
| **G** | **B** | **A** | **Y0** | **Y1** | **Y2** | **Y3** |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H= Logic High, L= Logic Low, X= Don’t Care

**Connection Diagram:**

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**Lab Tasks**

**Question 1:**Implement the following on logic trainer function using 4x1 mux

F (X, Y, Z) = m1 + m2 + m6 + m7

**Question 2:**Implementthe following on logic works:

Dual 2x1 MUX Using 2x1 MUX(s)only

**Question 3:**Implement the following on logic works

4x1 MUX using one 2x4 decoder, four ANDs and one OR gate